3-23-00

A

Patent Application Transmittal

(only for new nonprovisional applications under 37 C.F.R. 1.53(b))

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Date: March 22, 2000
Attorney Docket No.: 450100-3477.3

ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Sir:

With reference to the filing in the United States Patent and Trademark Office of an application for patent in the name(s) of:

Naoki FUJISAKI

entitled:

DIGITAL SERIAL DATA INTERFACE

X Continuing Application

X Continuation ___ Divisional ___ Continuation-in-Part (CIP) of prior application serial no. 08/879,116, filed June 19, 1997, which is a Continuation of application serial no. 08/493,732, filed June 22, 1995, now U.S. patent no. 5,903,569.

[Note: If priority under 35 U.S.C. 120 involves a series of respectively copending applications, then in this amendment identify each and its relationship to its immediate predecessor.]

X The prior application is assigned of record to SONY CORPORATION .

The following are enclosed:

X Specification (52 pages)

X 14 Sheet(s) of Drawings

X 9 Claim(s) (including 3 independent claim(s))

___ This application contains a multiple dependent claim

X Our check for $ 690.00 , calculated on the basis of the claims existing in the prior application (less any claims canceled herein) as amended by any enclosed preliminary amendment as follows:

Basic Fee, $690.00 ($345.00)	$ 690.00
Number of Claims in excess of 20 at $18.00 ($9.00) each:	-0-
Number of Independent Claims in excess of 3 at $78.00 ($39.00) each:	-0-
Multiple Dependent Claim Fee at $260.00 ($130.00)	-0-
Total Filing Fee	$ 690.00

___ Assignment Recording Fee $40.00 . . . . . -0-

___ This application is being filed within the month following the expiration of the term originally set therefor in the prior application. This is a petition to request a -month extension of time. A check covering the cost of the petition is enclosed.

Patent Application Transmittal

(only for new nonprovisional applications under 37 C.F.R. 1.53(b))

450100-3477.3

_X_ Oath or Declaration and Power of Attorney
___ New ___ signed ___ unsigned
_X_ Copy from a prior application (37 C.F.R. 1.63(d))

Deletion of Inventors

___ Signed Statement attached deleting inventor(s) named in the prior application (37 C.F.R. 1.63(d)(2) and 1.33(b))

Power of Attorney or Correspondence Address Change

_X_ Power of attorney and/or correspondence address was changed during prosecution of the prior application. The new power of attorney is to **William S. Frommer, Reg. No. 25,506** . The new correspondence address is indicated above.

_X_ Incorporation by Reference (for continuation or divisional application) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

_X_ A Preliminary Amendment is enclosed.
(Claims added by this amendment have been properly numbered consecutively beginning with the number next following the highest numbered original claim in the prior application.)

_X_ Cancel in this application original claims 2-21 of the prior application before calculating the filing fee. (At least one original independent claim must be retained for filing purposes.)

___ New formal drawings are enclosed.

_X_ Certified copy of each foreign priority application on which the claim for priority under 35 U.S.C. 119 is based was filed in prior U.S. application serial no. 08/493,732, filed June 22, 1995. A list of said foreign priority application(s) is provided below. Acknowledgement thereof is requested.

Application No.	Filed	In
6-144403	27 June 1994	Japan

Please charge any additional fees required for the filing of this application or credit any overpayment to Deposit Account No. 50-0320.

Respectfully submitted,

FROMMER LAWRENCE & HAUG LLP
Attorneys for Applicant
WILLIAM S. FROMMER

By: _____
Reg. No. 25,506

SONY\3477.3\3477-3.CON (WSF\GK\car)

PATENT
450100-3477.3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Naoki FUJISAKI

Continuation of Serial No.: 08/879,116

Filed : Herewith

For : DIGITAL SERIAL DATA INTERFACE

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Date of Deposit March 22, 2000

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" Service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

(Typed or printed name of person mailing paper or fee)

(Signature of person mailing paper or fee)

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Box Patent Application
Washington, D.C. 20231

Sir:

Before the issuance of the first Official Action, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Page 1, line 2, please insert:

--CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of pending prior application Serial No. 08/879,116, filed June 19, 1997, which is in turn a Continuation of application Serial No. 08/493,732, filed June 22, 1995, now U.S. Patent No. 5,903,569.--

IN THE CLAIMS:

Please cancel claims 1-21.

Please add the following claims:

--22. A serial digital data transmitting apparatus comprising:

digital packet generating means for generating a first digital packet conforming to the format for a second digital packet standard, said first digital packet comprising:

a payload portion into which digital data is inserted;

a first start synchronization code storage portion positioned at a preceding portion of said payload portion into which a start synchronization code is inserted, said start synchronization code indicating a start of said digital data inserted into said payload portion;

a first end synchronization code storage portion into which an end synchronization code is inserted, said end synchronization code indicating an end of said digital data inserted into said payload portion; and

an ancillary data storage portion positioned between said first end synchronization code storage portion and said first start synchronization code storage portion, and into which an ancillary data is inserted;

wherein said second digital packet comprises:

an active video portion corresponding to said payload portion into which video data is inserted;

a second start synchronization code storage portion corresponding to said first start synchronization code storage portion positioned at a preceding portion of said active video portion into which said start synchronization code is inserted, said start synchronization code indicating a start of said video data inserted into said active video portion;

a second end synchronization code storage portion corresponding to said first end synchronization code storage portion into which said end synchronization code is inserted, said end synchronization code indicating an end of said video data inserted into said active video portion; and

an auxiliary data storage portion corresponding to said ancillary data storage portion positioned between said second end synchronization code storage portion and said second start synchronization code storage portion, and into which auxiliary data is inserted;

said payload portion including one or more channels, each channel comprising a data portion into which said digital data is inserted and a type portion into which type data is

inserted, said type data being indicative of a type of said inserted digital data in said data portion; and

serial digital transmitting means for transmitting serial digital data translated by said digital packet into said serial digital data.

23. The serial digital data transmitting apparatus according to claim 22, wherein said digital data inserted in said data portion of said payload area is compressed video data.

24. The serial digital data transmitting apparatus according to claim 22, said second digital packet is defined by SMPTE-259M.

25. A serial digital data transmitting method comprising the steps of:

generating a first digital packet conforming to the format for a second, digital packet standard, said first digital packet comprising:

a payload portion into which digital data is inserted;

a first start synchronization code storage portion positioned at a preceding portion of said payload portion into which a start synchronization code is inserted, said start synchronization code indicating a start of said digital data inserted into said payload portion;

a first end synchronization code storage portion into which an end synchronization code is inserted, said end synchronization code indicating an end of said digital data inserted into said payload portion; and

an ancillary data storage portion positioned between said first end synchronization code storage portion and said first start synchronization code storage portion, and into which an ancillary data is inserted;

wherein said second digital packet comprises:

an active video portion corresponding to said payload portion into which video data is inserted;

a second start synchronization code storage portion corresponding to said first start synchronization code storage portion positioned at a preceding portion of said active video portion into which said start synchronization code is inserted, said start synchronization code indicating a start of said video data inserted into said active video portion;

a second end synchronization code storage portion corresponding to said first end synchronization code storage portion into which said end synchronization code is inserted, said end synchronization code indicating an end of said video data inserted into said active video portion; and

an auxiliary data storage portion corresponding to said ancillary data storage portion positioned between said second end synchronization code storage portion and said second start synchronization code storage portion, and into which auxiliary data is inserted;

said payload portion including one or more channels, each channel comprising a data portion into which said digital data is inserted and a type portion into which type data is

inserted, said type data being indicative of a type of said inserted digital data in said data portion;

translating said digital packet into serial digital data; and

transmitting said serial digital data.

26. The serial digital data transmitting method according to claim 25, wherein said digital data inserted in said data portion of said payload area is compressed video data.

27. The serial digital data transmitting method according to claim 25, said second digital packet is defined by SMPTE-259M.

28. A serial digital data signal, comprising:

a first digital packet conforming to the format for a second digital packet standard, said first digital packet comprising:

a payload portion into which digital data is inserted;

a first start synchronization code storage portion positioned at a preceding portion of said payload portion into which a start synchronization code is inserted, said start synchronization code indicating a start of said digital data inserted into said payload portion;

a first end synchronization code storage portion into which an end synchronization code is inserted, said end synchronization code indicating an end of said digital data inserted into said payload portion; and

an ancillary data storage portion positioned between said first end synchronization code storage portion and said first start synchronization code storage portion, and into which an ancillary data is inserted;

wherein said second digital packet comprises:

an active video portion corresponding to said payload portion into which video data is inserted;

a second start synchronization code storage portion corresponding to said first start synchronization code storage portion positioned at a preceding portion of said active video portion into which said start synchronization code is inserted, said start synchronization code indicating a start of said video data inserted into said active video portion;

a second end synchronization code storage portion corresponding to said first end synchronization code storage portion into which said end synchronization code is inserted, said end synchronization code indicating an end of said video data inserted into said active video portion; and

an auxiliary data storage portion corresponding to said ancillary data storage portion positioned between said second end synchronization code storage portion and said second start synchronization code storage portion, and into which auxiliary data is inserted;

said payload portion including one or more channels, each channel comprising a data portion into which said digital

data is inserted and a type portion indicative of a type of said inserted digital data in said data portion;

wherein said first digital packet is converted into serial digital data and is transmitted, and at least said stored ancillary data is used to direct the operation of a playback device.

29. The serial digital data transmitting signal according to claim 28, wherein said digital data inserted in said data portion of said payload area is compressed video data.

30. The serial digital data transmitting signal according to claim 28, said second digital packet is defined by SMPTE-259M.--

REMARKS

This preliminary amendment presents new claims 22-30. No new matter is added. Entry of the above new claims and early examination on the merits are respectfully requested.

Respectfully submitted,

FROMMER LAWRENCE & HAUG LLP
Attorneys for Applicant

By: _____
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SONY\3477.3\3477-3.PRE (WSF\GK\car)

Digital Serial Data Interface

FIELD OF THE INVENTION

This invention relates to a method and apparatus for transmitting and receiving a digital data signal in a digital data communication system, such as a local area network (LAN), or the like.

BACKGROUND OF THE INVENTION

Among the apparatus for handling and receiving speech signals or audio signals, there is video equipment, such as a television, or audio equipment, such as a radio, CD player, MD player or a video tape recorder (VTR). As a method for communication of signals employed in such apparatus, such as a video tape recorder (VTR), with other equipment, a serial digital interface (SDI) format is proposed by the Society of Motion Picture and Television Engineers (SMPTE) in *Proposed SMPTE Standard for Television-10-bit 4:2:2 Component and 4fsc Composite Digital Signals Serial Digital Interface* (SMPTE-295M, 1994 Revision-Seventh Draft, Febuary 16, 1994) as a standard for

digital audio and video signals. This SDI standard is basically a standard for signals governed by D-1 or D-2 formats for digital signals. The disclosure of Proposed SMPTE standard SMPTE-295M is hereby incorporated herein by reference.

Fig.1 shows a schematic arrangement of the SDI format which represents the application of D-1 format signals.

An upper part of Fig.1 shows a frame format of a frame made up of 1716 samples in the horizontal direction and 525 lines in the vertical direction. Digital video signals are placed in a first field active video section AVC_1 of 1440 horizontal samples and 244 vertical lines and a second field active video section AVC_2 of 243 lines. Specifically, the first field active video section AVC_1 is a digital video signal of odd fields and the second field active video section AVC_2 is a digital video signal of even fields. Ahead of the first field active video section AVC_1 and the second video active section AVC_2 are respectively inserted 9-line vertical blanking section VBK_1, VBK_2 and 10-line optional blanking sections OBK_1, OBK_2. Ahead and back of the first field active video section AVC_1, second video active section AVC_2, vertical blanking sections VBK_1, VBK_2 and the optional blanking sections OBK_1, OBK_2 are inserted a 4-sample

start synchronization code SAV indicating the start of an active line and a 4-sample end synchronization code EAV indicating the end of the active line. Between the start synchronization code SAV and the end synchronization code EAV are placed 268 samples of an ancillary data section ANC which are ancillary data for horizontal blanking. A mid part of Fig.1 indicates a signal of a frame format shown at the upper part of Fig.1 in a line format having a width of 10 bits. For transmitting signals of the SDI format, parallel/serial conversion and encoding of the transmission channel are carried out as shown at a lower part of Fig.1, and the signals are transmitted as serial signals having a data rate of 270 Mbps.

Although data transmission by the SDI format is achieved at a high speed, the SDI format is not suited as a transmission channel for variegated data, while it is possible to transmit only a limited type of data (information). Specifically, the data sorts capable of being transmitted include one channel of picture signals(or video signals) and 8 channels at most of speech signals (or audio signals) as the base band digital audio signals. Thus the SDI format is not suited to transmission and reception of plural channels of the same sort of data or channel

multiplication for coping with transmission and reception of plural sorts of data. On the other hand, data other than picture signals or speech signals are transmitted over a physically separate channel. In addition, the SDI format basically takes account only of one-to-one unidirectional data transmission.

In general, when simultaneously transmitting plural sorts of data, the method of providing a data transmission channel for each data sort is simple and easy, it being unnecessary to carry out data processing for transmitting excessive data. However, this presents a problem in efficiency and economic profitability in connection with cost involved in the entire data transmission system, cost involved in the data transmission channel, or labor in maintenance or extendibility of the data transmission system.

In local networks employed in data communication (LAN), especially in information processing equipment, data communication channels, such as Ethernet or token ring, have become popular in use. However, such data communication channel inherently has been developed as a data communication channel handling temporally discrete data, such as packet data emplcyed for an electronic computer, while it is not suited as a transmission channel for temporally continuous data, such as

picture/video or speech/audio signals, which require maintenance of a temporal relation between the transmitting and receiving sides. On the other hand, the data transmission rate of the data communication channel is rather low and is not suited to transmission of picture signals which require wide frequency range, or bandwidth.

The technological tendency in the near future is to digitize all kinds of the information, inclusive of the picture/video and speech/audio data, and to treat the information simply as a bitstream irrespective of the data type. Above all, in the future digital integrated network, exemplified by the AM technique, all kinds of data are transmitted as a multiplexed bitstream. If such technical tendency is taken into consideration, the SDI format currently standardized for picture signal transmission is not fully satisfactory, while there lacks at present a particular data format for multiplexing and transmitting various data and control signals among plural communication equipment.

SUMMARY OF THE INVENTION

In view of the foregoing, it is an object of the present

invention to provide a method and apparatus for transmitting and receiving a digital signal, whereby plural sorts, or types, of picture/video and speech/audio signals and the like may be transmitted as one bitstream.

In one aspect, the present invention provides a method for transmitting a digital signal in which a digital signal format of a transmitted digital signal is constituted by a first data portion made up of digital video data, a start synchronization code and an end synchronization code for bit synchronization for the first data portion, and an auxiliary data portion located between the start synchronization code and the end synchronization code and which is made up of plural split areas. Each of the split areas of the auxiliary data portion contains at least one of a type area indicating the data type, a byte count area indicating the data volume and a data area which is a second data portion made up of digital audio data.

At the leading end of the auxiliary data portion, there is provided a line number area indicating the line number of the data.

The auxiliary data portion contains an error correction code for detecting and correcting errors in data of the type area and

the byte count area.

The first data portion is made up of digital video data of a plurality of channels and the second data portion is made up of digital audio data of plurality of channels. Of course, the first data portion could also constitute audio data or other data. Likewise, the second data portion could constitute video or other data. The digital signal format contains transmission data and reception data used to identify and characterize the format and nature of the data being transmitted.

In another aspect, the present invention provides an apparatus for transmitting a digital signal having a plurality of data outputting media sources, a plurality of delay adjustment units for respectively adjusting the delay of the data from said media sources, a plurality of rate converting units for converting the data transmission rate of the respective data from the rate converting units into a transmission rate of a transmission channel, a plurality of attribute information processing units for appending the attribute information to the respective data from the rate converting units, a multi-media switching unit for optionally selecting data of the respective media sources from the attribute information processing units, a

transmission controlling unit for controlling the delay adjustment units, rate converting units, attribute information processing units and the multi-media switching unit, and a multiplexing unit for multiplexing plural data from the multi-media switching unit.

In a still another aspect, the present invention provides a device for receiving a digital signal having a demultiplexing unit for demultiplexing plural multiplexed data into media source based data, a demultiplexed media switching unit for switching plural data from the demultiplexing unit into respective suitable media channels, a plurality of attribute information processing units for processing the plural data switched by the demultiplexed media switching unit based upon the attribute information for these data, a plurality of rate converting units for converting the transmission rate of the respective data from the attribute information processing units into the playback rate for data reproduction, a plurality of delay adjustment units for adjusting the respective data from the plural rate conversion units into optimum delay amounts, and a plurality of media reproducing units for respectively reproducing the data from the delay adjustment units.

In yet another aspect, the present invention provides a digital signal transmission and reception device having the above-mentioned digital signal transmitting device and the above-mentioned digital signal receiving device on the signal transmitting and signal receiving sides, respectively.

With the method for transmitting the digital signal according to the present invention, the digital signal, such as digital video data or digital video data, is transmitted in a digital signal format interchangeable with the SDI format of the conventional digital signal transmitting method, that is a digital signal format having a first data portion made up of digital video data, a start synchronization code portion, an end synchronization code portion, and an auxiliary data portion. Each of the split areas of the auxiliary data portion contains at least one of a type area indicating the data type, a byte count area indicating the data volume, and a data area which is a second data portion made up of digital audio data. At the leading end of the auxiliary data portion, there is provided a line number area indicating the line number of the data, while the first data portion is made up of digital video data of plural channels and the second data portion is made up of digital audio

data of plural channels.

With the method for transmitting the digital signal, data from plural media are transmitted in the above-defined digital signal format. The transmitted data is received by a digital signal receiving device where data from plural media are reproduced.

The digital signal format proposed by the present invention assures upward compatibility with respect to a device for transmitting and receiving data of the conventional SDI format and hence has affinity, or compatibility, to the existing digital signal transmission system. In addition, past network resources may be directly exploited, while any newly arising cost may be minimized and the equipment employing the conventional SDI format may be introduced into another sort of network. It is also possible to interconnect a system exploiting the present digital signal transmitting method, a network or system such as existing computer network and an integrated digital network such as future ATM network in order to effect digital signal transmission between the interconnected systems.

By providing a line number area indicating the data line number at the leading end of the auxiliary data portion, an

optional number of line numbers can be set, so that asymmetrical digital signal transmission, such as 1:n transmission, becomes feasible in addition to the conventional 1:1 digital signal transmission.

By providing the auxiliary data portion having error correction code for error detection and correction for the type area data and the byte count area data, digital signals may be transmitted more correctly.

The first data portion is made up of digital video data of plural channels and the second data portion is made up of digital audio data of plural channels, so that multi-channel transmission of plural media data inclusive of encoded data may be realized on a sole transmission channel.

The digital signal format contains both the data for transmission and data for reception, so that sole media data may be bi-directionally transmitted by serial digital communication.

With the digital signal transmission device and the signal reception device of the present invention, the conventional SDI format employed in video equipment may be extended to a more variegated communication system for general digital data inclusive of base-band audio data and video data, thus enabling

more general digital communication. Since communication of plural media data is physically possible by a sole communication medium, system flexibility and hence system maintenance and management such as network modification may be improved significantly.

With the digital signal transmission/reception device of the present invention, since the arrangement of the digital signal reception device and that of the digital signal transmission device may be combined together, interconnection with a digital data network, such as an external computer, or a digitized public network, such as ISDN, as well as with a network between existing video equipment, may be facilitated, thus allowing it to realize reciprocal communication between all sorts of media easily and broadly. This provides a more intimate relation between networks and more efficient integration, separation, editing, management, maintenance and retrieval of plural media efficiently and in a short time irrespective of the contents of digitized data, thus enabling more flexible long-term network construction.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 illustrates a schematic arrangement of a conventional

SD1 format.

Fig.2 illustrates a schematic arrangement of a SD1 format according to the method for transmitting a digital signal according to the present invention.

Fig.3 illustrates a typical arrangement of a line format of the SDI format shown in Fig.1.

Fig.4a illustrates an illustrative construction of a line number area, type area and a byte count area.

Fig.4b illustrates an illustrative construction of a line number area, type area and a byte count area.

Fig.4c illustrates an illustrative construction of a line number area, type area and a byte count area.

Fig.5a illustrate a construction of a line number area for extension of the number of line numbers.

Fig.5b illustrate a construction of a line number area for extension of the number of line numbers.

Fig.5c illustrate a construction of a line number area for extension of the number of line numbers.

Fig.6a illustrate a schematic construction of a line format according to a first example of application of the SDDI format.

Fig.6b illustrate a schematic construction of a line format

according to a first example of application of the SDDI format.

Fig.7a illustrate a schematic arrangement of a 1:m broadcast communication system when employing a line format of the first example of application of Fig.6.

Fig.7b illustrate a schematic arrangement of a 1:m broadcast communication system when employing a line format of the first example of application of Fig.6.

Fig.7c illustrate a schematic arrangement of a 1:m broadcast communication system when employing a line format of the first example of application of Fig.6.

Fig.8a illustrate a schematic arrangement of a line format of the second example of application of the SDDI format.

Fig.8b illustrate a schematic arrangement of a line format of the second example of application of the SDDI format.

Fig.9a illustrate a schematic arrangement of a bidirectional communication system by m transmission and reception equipment when employing the line format of the second example of application of Fig.8.

Fig.9b illustrate a schematic arrangement of a bidirectional communication system by m transmission and reception equipment when employing the line format of the second example of

application of Fig.8.

Fig.9c illustrate a schematic arrangement of a bidirectional communication system by m transmission and reception equipment when employing the line format of the second example of application of Fig.8.

Fig.10 illustrates a schematic arrangement of a digital signal transmission and reception apparatus according to the present invention.

Fig.11 illustrates an arrangement of a digital signal transmission apparatus according to the present invention.

Fig.12 illustrates an arrangement of a digital signal transmission and reception apparatus according to the present invention.

Fig. 13 illustrates an embodiment of the present invention.

Fig. 14 illustrates an embodiment of the present invention.

Fig. 15 illustrates an embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to the drawings, preferred illustrative embodiments of the present invention will be explained in detail. Fig.2 illustrates a schematic arrangement of a signal format employing the method for digital signal transmission according to the present invention. Specifically, the signal format is termed a serial digital data interface (SDDI) format. The SDDI format shown in Fig.2 is an application of the D-1 format.

The SDDI format has a first data section DT_1 and a second data section DT_2. Ahead of the first data section DT_1 and the second data section DT_2 are inserted blank data sections BDT_1 and BDT_2, respectively. Ahead and back of the data sections DT_1 and DT_2 and the blank data sections BDT_1 and BDT_2 are put 4-sample start synchronization code SAV and 4-sample end synchronization code EAV, respectively. Between the start synchronization code SAV and the end synchronization code EAV is put an ancillary data section ANC, which is auxiliary data.

The present SDDI format, thus taking interchangeability with the conventional SDI format into account, represents extension of the SDI in some respects. Specifically, a frame format shown at an upper part of Fig.2, that is the blank data sections BDT_1 and BDT_2 of the format in the vertical direction, may be freely

changed as to the positions and the numbers of lines thereof by setting of the data type and the line numbers as later explained. Thus the blank data sections BDT_1 and BDT_2 may be set in the same manner as for the conventional SDI format. Consequently, with a system configuration in which signal switching may be made at a vertical blanking period by an existing lauter or switcher, SDDI format data may be employed in a form in which it is precompleted in units in the vertical blanking period. Also, depending on data setting, effective data may be inserted in the entire frame area to provide data sections DT_1, DT_2. Thus the SDDI format allows for flexible system construction.

The line format shown at a mid part of Fig.2, that is the horizontal format, is made up of a 4-sample end synchronization code EAV, 268-sample ancillary data section ANC, a 4-sample start synchronization code SAV and a 1440-sample payload section PAD. With the present SDDI format, similarly to the conventional SDI format, the start synchronization code SAV and the end synchronization code EAV are inserted, so that interchangeability may be maintained between signals of the SDDI format and those of the SDI format.

When transmitting signals of the SDDI format, similarly to

the transmission of the conventional SDI format signals, parallel-to-serial conversion and transmission channel coding are carried out and signal transmission occurs as serial signals having a data rate of, for example, 270 Mbps as shown at a lower part of Fig.2.

Fig.3 shows an illustrative constitution of the SDDI format.

At a leading end of the ancillary data section ANC is put a line number area LN indicating the number to which belongs the line data, as shown at an upper part of Fig.3. By setting the line number, the vertical blanking domain of a particular line number can be regenerated, as in the case of the conventional SDI format. Within the ancillary data section ANC can be put audio data and control data of plural channels, such as audio data areas AD_1 or AD_2 or control data area CD_1, in a mixed state. Also, data of one channel can occupy data areas of a variable length based upon respective transmission rates of plural sorts of data. Specifically, the audio data area AD or the control area data CD are combined with flags FG to constitute one-channel data. Such one-channel data may be constituted by a flag FG_1, an audio data area AD_1, a flag FG_2, an audio data area AD_2, a flag FG_3, a control data area CD_1, a flag FG_4, ...as shown for example at

Fig.3.

One data channel is made up of a type area TP, a byte count area BC, an error correction code ECC and a data area DT, as shown at a mid part of Fig.3. The type area TP denotes the contents of data of the data area DT, while the byte count area BC denotes the length of data of the data area DT. The error correction code ECC includes a check sum or a cyclic redundancy code (CRC) of the type area TP and the byte count area BC. By the error correction code ECC, error detection and correction is carried out of the type area TP and the byte count area BC.

Within the payload section PAD can be put video data of plural channels in a mixed state. The video data of the respective channels is made up of flags FG and video areas VD. Thus the video data is constituted by a flag FG_1, a video data area VD_1, a flag FG_2, a video data area VD_2, a flag FG_3, a video data area VD_3, a flag FG_4, a video data area VD_4, flag FG_5, ...as shown at a lower part of Fig.3. One data channel is made up of a type area TP, a byte count area BC, an error correction code ECC and a data area DT, similarly to the constitution of the data channel in the ancillary data section ANC, as shown at a lower part of Fig.3.

The detailed arrangement of the line number area LN, type area TP and the byte count area BC is shown in Figs.4a, 4b and 4c, respectively.

The line number area LN is made up of 10 bits and indicate the line number by 7 bits, that is bit 0 (LN0) up to bit 6 (LN6). Bit 7 or LCY is a bit for extension of the line number area and indicates whether or not the line number area LN has been extended. Bit 8 and bit 9 indicate an even number parity of the values from bit 0 to bit 7 and an inversion of the bit 8, respectively.

The number of the line number areas LN may be increased by setting the bit 7, if necessary, as described above. The illustrative construction of the line number area at the time of extension of the number of line numbers is shown in Fig.5A, Fig. 5B & Fig. 5C. If the bit 7 of the line number area LN is 0, as shown in Fig. 5A, the line number area LN is not extended and the line number is indicated solely by the line number area LN. However, if the bit 7 of the first line number area LN_1 is 1, as shown at a mid part of Fig.5B, the next 1-word area, made up of 10 bits, is also an area indicating the line number, that is a line number area LN_2. Referring to Fig.5b, since bit 7 of the

line number area LN_2 is 0, the region up to the bit 7 becomes the line number area LN. The line number area may be extended by two words, as shown in Fig.5c. In this case, the line number is denoted using LN0 to LN20 by bits 0 to 6 of the line areas LN_1 LN_2 and LN_3. An optional number of line numbers may be set by extending the line number area LN in this manner.

The type area shown in Fig.4b and the byte count area shown in Fig.4c are defined as header data for data. Thus the type area TP denotes the contents of data by the values of from T0 of bit 0 to T6 of bit 6. Data types are defined depending on the data sorts, such as type '00' for audio data of the MPEG system and for video data of the MPEG system, respectively. By defining data types of invalid data, such as blank data, it becomes possible to set a line corresponding to the vertical blanking domain, while it also becomes possible to cope with a system of switching the signals on the field basis, such as an existing lauter or a switcher. The byte count area BC denotes the length of the next following data area DT by the values of BC0 of bit 0 to BC6 of bit 6. Similarly to the line number area LN, both the type area TP and the byte count area BC can be extended depending on the value of the extension bit of bit 7 thus

enabling flexible area setting. Meanwhile, the bit 8 of the type area TP and bit 8 of the byte count area BC are even-number parities of the values of bit 0 to bit 7, while bit 9 of the type area TP and bit 9 of the byte count area BC are inverted values of the bits 8.

If, with the above-described SDDI format, the signals of the ancillary data section ANC and the payload section PAD are replaced by signals of the D-1 format, the resulting format is the conventional D-1 format itself, thus assuring complete interchangeability between the SDDI format signals and the SD1 format signals.

An example of a first application of the method for digital signal transmission is shown in Fig.6A and Fig.6B.

In the first example of application, each of the ancillary data section and the payload section in the SDDI format is divided into data having n sub-areas, as shown in Fig.6a. Alternatively, the entire area excluding the start synchronization code SAV and the end synchronization code EAV is divided into data having n sub-areas, as shown in Fig.6b. If, when the area is divided into n sub-areas in the SDDI format, as with the present first example of application, each of data

communication equipment having a 1:m connection employs each 1/n sub-area, it becomes possible to achieve n-channel broadcast type data communication between a data transmission equipment and m data reception equipment. The interconnection between the data transmission equipment T and the m data reception equipment may be of a star shape as shown in Fig.7A, a bus type as shown in Fig.7b or of a ring type as shown in Fig.7c. It is also possible for the m data reception equipment to receive data of a desired one of n sub-areas or to perform communication service of receiving data of synchronous reception of data of a specified sub-area.

A second example of application of the method for digital signal transmission is shown in Fig.8A and Fig. 8B.

With the present second example of application, each of the ancillary data section and the payload section in the SDDI format is divided into data having n sub-areas, with the ancillary section being used as a channel for data transmission and the payload section being used as a channel for data reception, as shown in Fig.8a. Alternatively, each area is time-multiplexed so as to be used for transmission and reception each by 1/n of the channel time, as shown in Fig.8b. If the area in the SDDI format

is divided into n sub-areas dedicated to transmission and reception, it becomes possible to achieve bidirectional serial digital data communication between desired two of interconnected m data transmission/reception equipment. The interconnection between the data transmission equipment T and the m data reception equipment may be of a star shape as shown in Fig.9a, a bus type as shown in Fig.9b or of a ring type as shown in Fig.9c.

If, with the above-described examples of application, an accessing method is taken into consideration, it becomes possible to carry out data communication equivalent to LAN which performs data transmission by exchange of packet data such as Ethernet or the token ring, or network data communication of the sub-area (band) appointment type network exchange system convenient for temporally continuous data communication such as picture or speech as employed in a usual telephone network. Also, it becomes possible to achieve a high-speed broad-range network.

A schematic arrangement of a digital signal transmission and reception apparatus, employing the above-described method for digital signal transmission, is shown in Fig.10.

The basic data flow on the transmission side 100 of the digital signal transmission and reception device is symmetrical

with respect to its reception side. That is, the transmission side 100(transmitter) serially transmits signals multiplexed from data from a desired media source, while the reception side receives and reproduces the serially transmitted signals from the media source.

In one embodiment of the present invention, the transmission side 100, or encoder, incorporates a plurality of input channels for receiving and processing data from a pluraltiy of media sources(media source data). The transmitting, or transmission, side 100 receives the media source data from media sources 1_1 to 1_n and transmits it to delay adjustment units 2_1 to 2_n, respectively. The delay adjustment units 2_1 to 2_n delay the output of the different media data by a predetermined amount as part of the process of getting all data to flow at a common data transmission rate. Output data of the delay adjustment units 2_1 to 2_n are transmitted to rate conversion units (data transmission rate converters) respectively. The rate conversion units 3_1 to 3_n convert the data transfer rates of the input data into the rate of transmission on the communication transmission channel(network). In other words, the data transmission rate is converted to a common data transmission rate. The media data,

rate-converted by the rate conversion units 3_1 to 3_n, are subsequently transmitted to attribute information processing units (attribute data processors) 4_1 to 4_n, respectively. The attribute information processing units 4_1 to 4_n append subsidiary data, or attribute data, to the respective media data. The appended attribute data may be the above-mentioned type area data or the byte count data in the SDDI format as previously explained. The data having the attribute data appended thereto in the attribute data processing units 4_1 to 4_n are transmitted to a multi-media switching unit 5. The multi-media switching unit 5 optionally or alternately selects plural data from the media data output from the attribute processors and transmits the selected data to a multiplexing unit (multiplexor) 7.

A transmission control unit 6 transmits the control information to the delay adjustment units 2_1 to 2_n, rate conversion units 3_1 to 3_n, attribute information processing units 4_1 to 4_n and to a multi-media switching unit 5, and causes processing to be performed in the delay adjustment units 2_1 to 2_n, rate conversion units 3_1 to 3_n, attribute information processing units 4_1 to 4_n and in multi-media switching unit 5 based upon the control information. The multiplexing unit 7 multiplexes

transmitted data from the attribute data processor into a serial signal which then is transmitted to a communication transmission channel, such as a communication network/LAN.

The receiving, or reception, side 200(receiver) receives the transmitted multiplexed data and transmits the received data to a separating unit (De-multiplexor) 8. The separating unit 8 demultiplexes the multiplexed serial data of plural media into the media data. The plural media-based data are transmitted to a demultiplexed media switching unit 9. The demultiplexed media switching unit 9 switches the transmitted media-based data to the appropriate media channel to transmit the data to attribute information processing unit (attribute data decoder) associated with the suitable media channels in attribute information processing units 10_1 to 10_n. Using the attribute information in the transmitted data, the attribute information processing units 10_1 to 10_n carry out required processing and conversion and subsequently delete the attribute information from the data. Part of the attribute information is routed to a reception controlling unit 14 so as to be used for control in the reception controlling unit 14.

Output data of the attribute information processing units

10_1 to 10_n are routed to rate conversion units (data transmission rate converters) 11_1 to 11_n. Since the data rate is the rate of transmission of the communication transmission channel, the rate conversion units 11_1 to 11_n convert the data rate to a rate matched to data reproduction of the respective media data. The rate-converted data are routed to delay adjustment units 12_1 to 12_n. The delay adjustment units 12_1 to 12_n perform delay processing most suited to the media on the transmitted data. These data are routed to and reproduced in the media reproducing units 13_1 to 13_n. The reception control unit 14 routes the control information to the demultiplexing media switching unit 9, attribute information processing units 10_1 to 10_n, rate conversion units 11_1 to 11_n and to the delay adjustment units 12_1 to 12_n. Processing by the demultiplexing media switching unit 9, attribute information processing units 10_1 to 10_n, rate conversion units 11_1 to 11_n and to the delay adjustment units 12_1 to 12_n is carried out based upon the transmitted control information.

As an illustrative example of the above-described digital signal transmission and reception device, a digital signal transmission and reception device for transmitting the encoded digital video signals, digital audio signals and non-compacted

digital audio data is hereinafter explained.

An illustrative arrangement of a digital signal transmission device within the digital signal transmission and reception device is shown in Fig.11.

From a picture encoding device 15, an audio encoding device 16 and an audio signal input unit 17 of Fig.11, there are supplied encoded media source data such as video data, encoded audio data and non-compacted audio data, respectively, sampled by sampling clock signals from a picture clock generator 18 generating sampling clock signals for data of the respective media, an audio clock oscillator 19 and sampling clock signals from an audio sampling oscillator 20. The sampling clocks generated by the audio clock generator 19 and the audio sampling oscillator 20 are derived from the sampling clock signals of the video data generated by the picture clock generator 18. The audio sampling oscillator 20 generates sampling clock signals based upon clock signals from the audio clock generator 19.

The encoded video data, encoded audio data and non-compacted audio data from the respective media are fed to delay processing FIFO memories 22, 23 and 24 adapted for adjusting the media-based delay caused by processing, such as encoding. The delay

processing FIFO memories 22 to 24 are fed with sampling clock signals from the picture clock oscillator 18, audio clock oscillator 19 and the audio sampling oscillator 20, respectively. Thus the encoded video data, encoded audio data and non-compacted audio data from the respective media are delayed to the extent required for the respective data, under control by a transmission control unit 21, so as to be written in the delay processing FIFO memories 22 to 24, based upon the input sampling clock signals, respectively. The respective media data are matched in time phase by the delay processing.

The encoded video data in the delay processing FIFO memory 22 and the encoded audio data in the delay processing FIFO memory 23 are subsequently read out based upon the sampling clock signals from the picture clock oscillator 18 and the audio clock generator 19 so as to be written in rate conversion FIFO memories 25 and 26, respectively. The data written in the rate conversion FIFO memories 25 and 26 are read out based upon transmission clock signals, that is clock signals generated by a transmission clock generator 27, so as to be sampled at the transmission rate and processed with rate conversion. The rate-converted data from the rate converting FIFO memories 25 and 26 are routed to header

data appending units 28 and 29, respectively. The header data appending units 28 and 29 append header data required for the respective data.

The non-compacted audio data in the delay processing FIFO memory 24 are routed to a rate converting and audio data flag appending unit 30 which is also fed with clock signals from the transmission clock generator 27. The data rate conversion and data appendage such as appendage of audio data flags, are collectively carried out at the rate converting and audio data flag appending unit 30.

A multi-media switching unit 31 selects one of the output encoded audio data from the header data appending unit 29 and the non-compacted audio data outputted from the rate converting and audio data flag appending unit 30. The audio data as selected by the multi-media switching unit 31 and the output encoded video data from the header data appending unit 28 are multiplexed in a multiplexing unit 32, using clock signals from the transmission clock generator 27. The resulting multiplexed serial signals are transmitted to a transmission encoding and outputting unit 33. The transmission encoding and outputting unit 33 performs appropriate transmission channel encoding on the transmitted

multiplexed data and outputs the processed data to a communication network.

The transmitted data is received and reproduced by a digital signal reception device shown in Fig.12.

The transmitted data is first received by a transmission decoding and reception unit 34 of Fig.12 and transmission channel decoded so as to be then supplied to a demultiplexing unit 35. The demultiplexing unit 35 demultiplexes the transmitted data to respective media-based data. Simultaneously, the transmission clock signal data are routed to a reception clock reproducing unit 36 where transmission clock signals are reproduced. From the reproduced transmission clock signals are derived the above-mentioned reproducing clock signals generated by a picture clock generator 40, a sound clock oscillator 41 and a sound sampling oscillator 42 inputting the reproducing clock signals to a picture decoding device 37, an audio decoding device 38, an audio decoding device 38 and an acoustic signal outputting unit 39.

Of the media-based audio data, demultiplexed by the demultiplexing unit 35, the audio data is transmitted to a demultiplexed media switching unit 43. The demultiplexed media switching unit 43 changes over the transmitted audio data by the

encoded audio data or the non-compacted audio data so that the encoded audio data and the non-compacted audio data are transmitted to a header data processing unit 44 and to a rate converting and audio data flag processing unit 45, respectively.

The header data processing unit 44 performs data processing using header data of the transmitted encoded audio data. The header data is simultaneously transmitted to a reception control unit 49. The processed data is written in a rate converting FIFO memory 46, based on the transmission clock signals from the reception clock reproducing unit 36, and is subsequently read out based upon the reproducing clock signals from the audio clock oscillator 41, under control by the reception controlling unit 49, in order to perform rate conversion on the sampling clock signals of the encoded audio data. The rate converting and audio data flag processing unit 45 collectively processes the transmitted non-compacted audio data with data rate conversion based upon the reproducing clock signals from the sound sampling oscillator 42 and with data processing employing the audio data flag.

The rate-converted data from the rate converting FIFO memory 46 and the processed data from rate converting and audio data

flag processing unit 45 are written in delay adjustment FIFO memories 47 and 48, based upon the reproducing clock signals from the audio clock oscillator 41. The delay adjustment FIFO memories 47 and 48 are controlled by the reception controlling unit 49 for delay adjustment among the respective media taking into account the delay caused in the respective media due to decoding. Thus the data adjusted for delay is read out from the delay adjustment FIFO memories 47 and 48 based upon the reproducing clock signals from the sound clock oscillator 41 so as to be transmitted to the audio decoding device 38 and the audio signal outputting unit 39.

The transmitted encoded audio data is decoded by the audio decoding device 38 to reproduce digital audio data. Digital audio data is also outputted from the audio signal output 39.

The video data demultiplexed by the demultiplexing unit 35 is transmitted to a header data processing unit 50. The header data processing unit 50 performs data processing using header data of the transmitted encoded video data. The header data information is also supplied to the reception controlling unit 49. The processed data is written in a rate converting FIFO memory 51, based upon transmission clock signals from the reception clock

reproducing unit 36, and is subsequently read out based upon the reproducing clock signals from the picture clock oscillator 40 under control by the reception controlling unit 49, for rate converting the sampling clock signals of the encoded video data. The rate converted data from the rate converting FIFO memory 51 is written in a delay adjustment FIFO memory 52 based on the playback clock signals from the picture clock oscillator 40. The delay adjustment FIFO memory 52 is controlled by the reception controller 49 as to delay adjustment among the respective media taking into account the delay introduced by e.g., decoding for the respective media. Thus the delay- adjusted data is read from the delay adjustment FIFO memory 52, based upon the reproducing clock signals from the picture clock oscillator 40, so as to be supplied to the picture decoding device 37. The picture decoding device 37 decodes the transmitted encoded video data for reproducing digital video data.

Another embodiment of the present invention is shown in Fig. 13 . This embodiment incorporates a sensor 800 for reading data, such as video data 810, audio data 820, graphic data or text data, from an optical disc recording medium 840 such as, for example, a digital video disc, compact disc, mini disc or the

like. A transmitter 830,such as that described in Fig.10, is included to accomodate each type of data read from the optical disc, and to process the data read from the optical disc to append header or attribute data and to convert the data transmission rate of each type of input data to a common data transmission rate. One example of this embodiment includes a video camera or imager and recorder device for recording video or audio data onto the optical recording medium.

Another embodiment is shown in Fig. 14 and includes a magnetic reproducing head 900 for reading data recorded on a magnetic recording medium 940 such as, for example, a magnetic tape or disc. The signal read from the magnetic recording medium (video data signal 910 and audio data signal 920) is then passed to a transmitter 930 such as that described in Fig. 10, where it is then processed to add header or attribute data and to convert the data tranmission rate to a common, predetermined data transmission rate. One example of this embodiment includes a video camera or imager and recorder device for recording video or audio data onto the magnetic recording medium.

A further embodiment of the present invention is shown in Fig. 15. Data, such as video, audio or text data, from a

plurality of various sources are input and received by the encoder (ENC) 1500, which transforms input data from one predetermined format into an output signal of another predetermined format at predetermined data transmission rate. Encoder 1500, performs the function of the transmission side 100 previously described herein. The output of Encoder 1500 is then provided to an input router 1510 which is controlled by Server Management System controller(SMS) 1520. The output from input router 1510 is directed to Server Data Controller (SDC) 1530 which directs the input data from Input router 1510 to a recorder/player MOD 1540 for selectively recording the input data onto a recording medium 1550, such as an Magneto Optical disk. Recorder/Player 1540 also performs the function of reading data recorded on a recording medium 1550 and outputting same to an output router 1560. Output router 1560 then outputs the data read from recording medium 1550 to a decoder section (DEC) 1570 which performs the functions of the receiving side 200 previously described herein. Output data from decoder 1570 can then be routed to any number of devices, including reproduction devices for the various data formats, or editing equipment for selectively compiling data into a desired sequence or form.

In view of the above description of the present invention, it will be appreciated by those skilled in the art that many variations modifications and changes can be made to the present invention without departing from the spirit or scope of the present invention as defined by the appended claims hereto. All such variations, modifications or changes are fully contemplated by the present invention.

WHAT IS CLAIMED IS:

1. A method of transmitting a digital signal comprising the steps of:

assembling a data packet comprised of a first data portion, a start synchronization code and an end synchronization code for bit synchronization for said first data portion, and an auxiliary data portion located between said start synchronization code and said end synchronization code ;

said auxilliary data portion comprises a type area indicating data type of said first data portion; and

transmitting said data packet via a communications network.

2. A method of transmitting a digital signal according to claim 1 wherein said first data portion comprises video data.

3. A method of transmitting a digital signal according to claim 1 wherein said first data portion comprises audio data.

4. A method of transmitting a digital signal according to claim 1 wherein said auxilliary data portion comprises a byte count

area indicating data volume.

5. A method of transmitting a digital signal according to claim 1 wherein said auxilliary data portion comprises a second data portion.

6. The method as claimed in claim 1 wherein line number area indicating the line number of data is provided at the leading end of said auxilliary data portion.

7. The method of claim 1 wherein said auxilliary data portion comprises error correction code data for detecting and correcting errors in data of said type area and said byte count area.

8. The method of claim 4 wherein said auxilliary data portion comprises error correction code data for detecting and correcting errors in data of said byte count area.

9. The method of claim 1 wherein said first data portion comprises digital video data and said second data portion comprises digital audio data.

9. The method as claimed in claim 1 wherein the digital signal format contains transmission data and reception data.

10. An apparatus for transmitting a digital signal comprising:

plurality of data outputting media sources;

plurality of delay adjustment units for respectively adjusting the delay of the data from said media sources;

plurality of rate converting units for converting the data transmission rate of the respective data from the rate converting units into a transmission rate of a transmission channel;

plurality of attribute information processing units for appending the attribute information to the respective data from said rate converting units;

multi-media switching unit for optionally selecting data of the respective media sources from the attribute information processing units;

transmission controlling unit for controlling said delay adjustment units, rate converting units, attribute information processing units and said multi-media switching unit; and

multiplexing unit for multiplexing plural data from said multi-media switching unit.

11. A device for receiving a digital signal comprising:

demultiplexing unit for demultiplexing plural multiplexed data into media source based data;

a demultiplexed media switching unit for switching plural data from the demultiplexing unit into respective suitable media channels;

a plurality of attribute information processing unit for processing the plural data switched by said demultiplexed media switching unit based upon the attribute information for these data;

a plurality of rate converting units for converting the transmission rate of the respective data from the attribute information processing units into the playback rate for data reproduction;

a plurality of delay adjustment units for adjusting the respective data from the plural rate conversion units into optimum delay amounts; and

a plurality of media reproducing units for respectively reproducing the data from the delay adjustment units.

12. A digital signal transmitting and receiving system

comprising:

a transmitting side;

a receiving side;

said transmitting side comprises a plurality of data outputting media sources, a plurality of delay adjustment units for respectively adjusting a delay of the transmission of data from said media sources, a plurality of rate converting units for converting the data transmission rate of the respective data output from said rate converting units into a transmission rate of a transmission channel, a plurality of attribute information processing units for appending the attribute information to the respective data from said rate converting units, a multi-media switching unit for optionally selecting data of the respective media sources from the attribute information processing units, a transmission controlling unit for controlling said delay adjustment units, rate converting units, attribute information processing units and the multi-media switching unit, and a multiplexing unit for multiplexing plural data from said multi-media switching unit; and

said receiving side comprises demultiplexing unit for demultiplexing plural multiplexed data to produce media source

based data,demultiplexed media switching unit for switching plural data from said demultiplexing unit into respective suitable media channels, a plurality of attribute information processing unit for processing the plural data switched by said demultiplexed media switching unit based upon the attribute information for these data, a plurality of rate converting units for converting the transmission rate of the respective data from the attribute information processing units into the playback rate for data reproduction, a plurality of delay adjustment units for adjusting the respective data from said rate conversion units into optimum delay duration, a plurality of media reproducing units for respectively reproducing data from said delay adjustment units.

13. A digital signal transmission system comprising:

a transmitter for transmitting digital signals;

a receiver for receiving digital signals transmitted from said transmitter;

said transmitter comprises:

a plurality of input channels for receiving data from anyone of a plurality of predetermined media sources;

each of said plurality of input channels comprise:

an input for receiving media source data from a predetermined media source at a predetermined data transmission rate;

first delay for delaying said media source data by a predetermined duration before outputting same to a first data transmission rate converter;

said first data transmission rate converter converts the transmission rate of said media source data from said predetermined data transmission rate to a common data transmission rate and outputs same to a first attribute data processor;

said first attribute data processor appends predetermined attribute data to said media source data and outputs same;

multiplexor for multiplexing the output from said plurality of input channels and outputting a multiplexed signal at a common data transmission rate to a communication network;

switcher for alternately routing said output from said attribute data processors of each of said plurality of input channels to said multiplexor;

said receiver comprises:

demultiplexor for receiving a multiplexed data signal at a common data transfer rate from said communication network and demultiplexing said multiplexed signal to produce a plurality of data signals and output same to a plurality of output channels;

each of said output channels comprise:

second attribute data decoder for decoding attribute data appended to said data signal;

second data transmission rate convertor for converting the data transmission rate of a said data signal from said common data transmission rate to a predetermined data transmission rate and outputting same to a second delay; and

said second delay provides a predetermined delay to said data signal before outputting same to a predetermined media reproduction device.

14. A digital signal transmitting device according to claim 13 wherein said media sources comprise video data sources.

15. A digital signal transmitting device according to claim 13 wherein said media sources comprise audio data sources.

16. A digital signal transmitting device comprising:

a first and second input channel for receiving data from a first and a second predetermined media source, respectively;

each of said first and second input channels comprise:

an input for receiving media source data from a predetermined media source at a predetermined data transmission rate; delay for delaying said media source data by a predetermined duration before outputting same to a data transmission rate converter; said data transmission rate converter converts the transmission rate of said media source data from said predetermined data transmission rate to a common data transmission rate and outputs same to an attribute data processor; said attribute data processor appends predetermined attribute data to said media source data and outputs same;

multiplexor for multiplexing the respective outputs from said first and second input channels and outputting a multiplexed signal at a common data transmission rate to a communication network;

switcher for alternately routing said outputs from said attribute data processors of said first and second input channels to said multiplexor;

said first predetermined media source comprises a video data source; and

said second predetermined media source comprises an audio data source.

17. A digital data signal receiver comprising:

demultiplexor for receiving a multiplexed data signal at a common data transfer rate from a communication network, and demultiplexing said multiplexed signal to produce a plurality of data signals and output same to a plurality of output channels;

each of said output channels comprise attribute data decoder for decoding attribute data appended to each of said data signals; data transmission rate convertor for converting the data transmission rate of a said data signal from said common data transmission rate to a predetermined data transmission rate and outputting same to a second delay; and

said delay provides a predetermined delay to said data signal before outputting same to a predetermined media reproduction device.

18. A digital signal transmission device comprising:

sensor for reading data recorded on an optical disc media to produce an audio media source data signal and a video media source data signal;

transmitter comprising a first and a second input channel for receiving said audio signal and said video signal from said sensor, respectively;

said first and second input channels each comprise an input for receiving an input signal at a predetermined data transmission rate; delay for delaying said input signal by a predetermined duration before outputting same to a data transmission rate converter; said data transmission rate converter converts the transmission rate of said input signal from said predetermined data transmission rate to a common data transmission rate and outputs same to an attribute data processor; said attribute data processor appends predetermined attribute data to said input signal and outputs same;

multiplexor for multiplexing the respective outputs from said first and second input channels and outputting a multiplexed signal at a common data transmission rate to a communication network; and

switcher for alternately routing said outputs from said attribute data processors of said first and second input channels to said multiplexor.

19. A digital signal transmission device comprising:

reproducing head for reading data recorded on a magnetic recording medium to produce an audio media source data signal and a video media source data signal;

transmitter comprising a first and a second input channel for receiving said audio signal and said video signal from said sensor, respectively;

said first and second input channels each comprise:

an input for receiving an input signal at a predetermined data transmission rate; delay for delaying said input signal by a predetermined duration before outputting same to a data transmission rate converter; said data transmission rate converter converts the transmission rate of said input signal from said predetermined data transmission rate to a common data transmission rate and outputs same to an attribute data processor; said attribute data processor appends predetermined attribute data to said input signal and outputs same;

multiplexor for multiplexing the respective outputs from said first and second input channels and outputting a multiplexed signal at a common data transmission rate to a communication network; and

switcher for alternately routing said outputs from said attribute data processors of said first and second input channels to said multiplexor.

20. A data transmission device according to claim 19, wherein said magnetic recording medium comprises a magnetic disc medium.

21. A data transmission device according to claim 19, wherein said magnetic recording medium comprises a magnetic tape medium.

ABSTRACT

A method and apparatus for digital signal transmission, in which data of plural media is transmitted and received over a communication transmission channel. A digital signal format for the transmitted digital signal has an ancillary data section ANC within which there are a plurality of channels for audio signals, each channel including a leading line number area LN, a type area TP, a byte count area BC, an error correction code ECC and a data area DT. The digital signal format also has a payload section PAD within which there are a plurality of channels for video signals, or the like. Each channel includes a type area TP, a byte count area BC, an error correction code ECC and a data area DT.

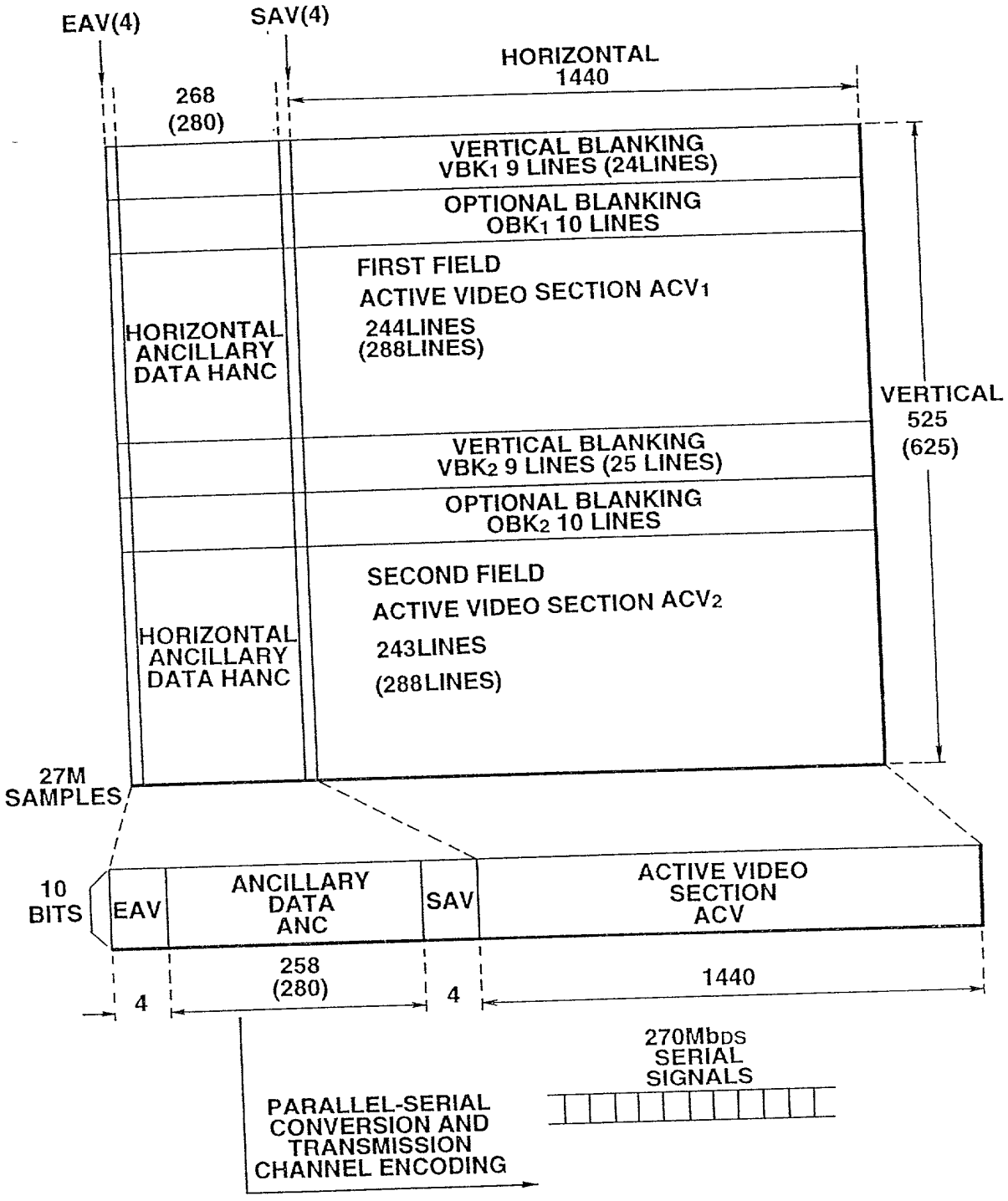
EAV(4)
SAV(4)
HORIZONTAL
1440
268
(280)
VERTICAL BLANKING
VBK1 9 LINES (24LINES)
OPTIONAL BLANKING
OBK1 10 LINES
FIRST FIELD
ACTIVE VIDEO SECTION ACV1
244LINES
(288LINES)
HORIZONTAL
ANCILLARY
DATA HANC
VERTICAL
525
(625)
VERTICAL BLANKING
VBK2 9 LINES (25 LINES)
OPTIONAL BLANKING
OBK2 10 LINES
SECOND FIELD
ACTIVE VIDEO SECTION ACV2
243LINES
(288LINES)
HORIZONTAL
ANCILLARY
DATA HANC
27M
SAMPLES
10
BITS
EAV
ANCILLARY
DATA
ANC
SAV
ACTIVE VIDEO
SECTION
ACV
258
(280)
1440
4
4
270Mbps
SERIAL
SIGNALS
PARALLEL-SERIAL
CONVERSION AND
TRANSMISSION
CHANNEL ENCODING

FIG.1

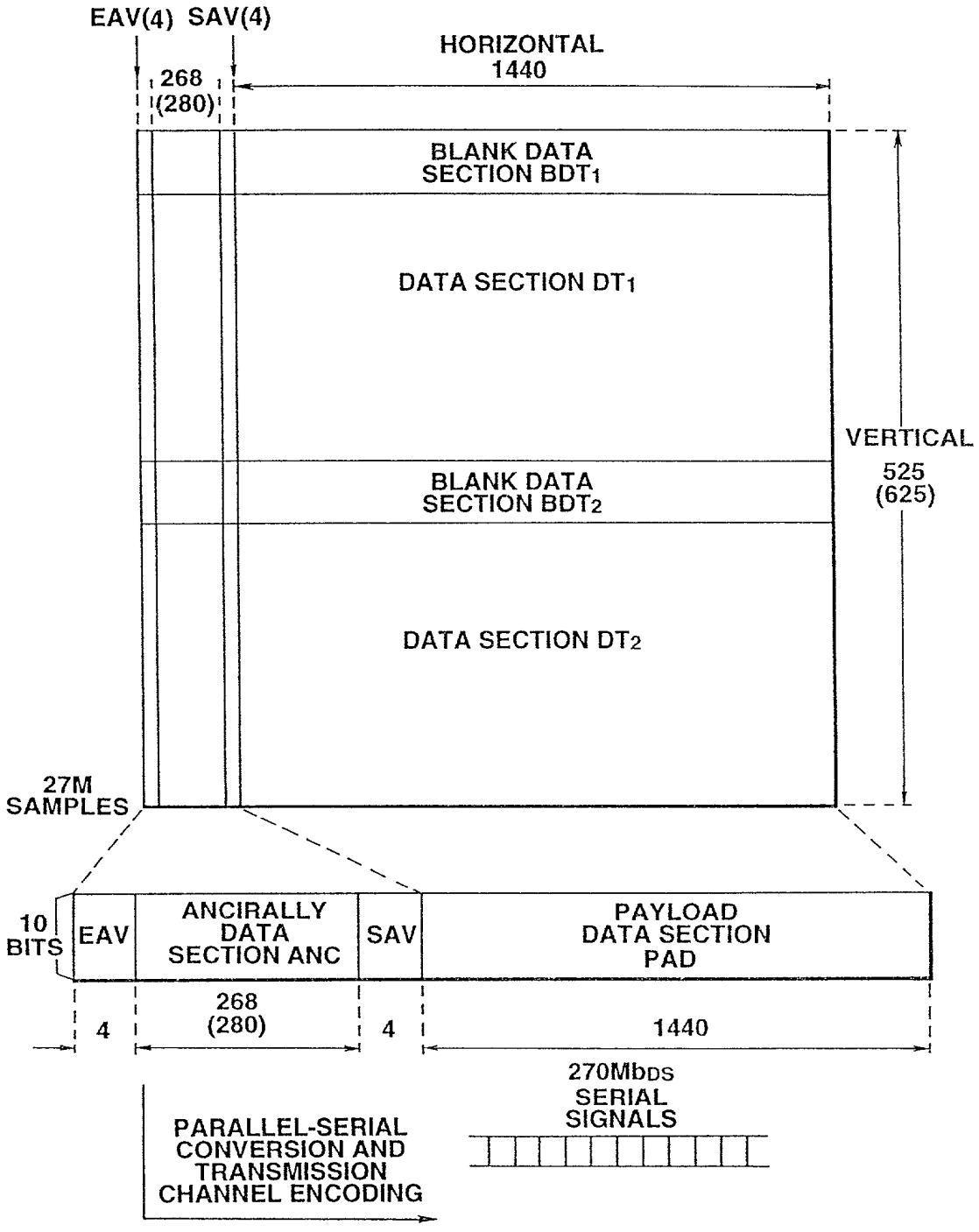
EAV(4)
SAV(4)
HORIZONTAL
1440
268
(280)
BLANK DATA
SECTION BDT1
DATA SECTION DT1
BLANK DATA
SECTION BDT2
DATA SECTION DT2
VERTICAL
525
(625)
27M
SAMPLES
10
BITS
EAV
ANCIRALLY
DATA
SECTION ANC
SAV
PAYLOAD
DATA SECTION
PAD
4
268
(280)
4
1440
270Mbps
SERIAL
SIGNALS
PARALLEL-SERIAL
CONVERSION AND
TRANSMISSION
CHANNEL ENCODING

FIG.2

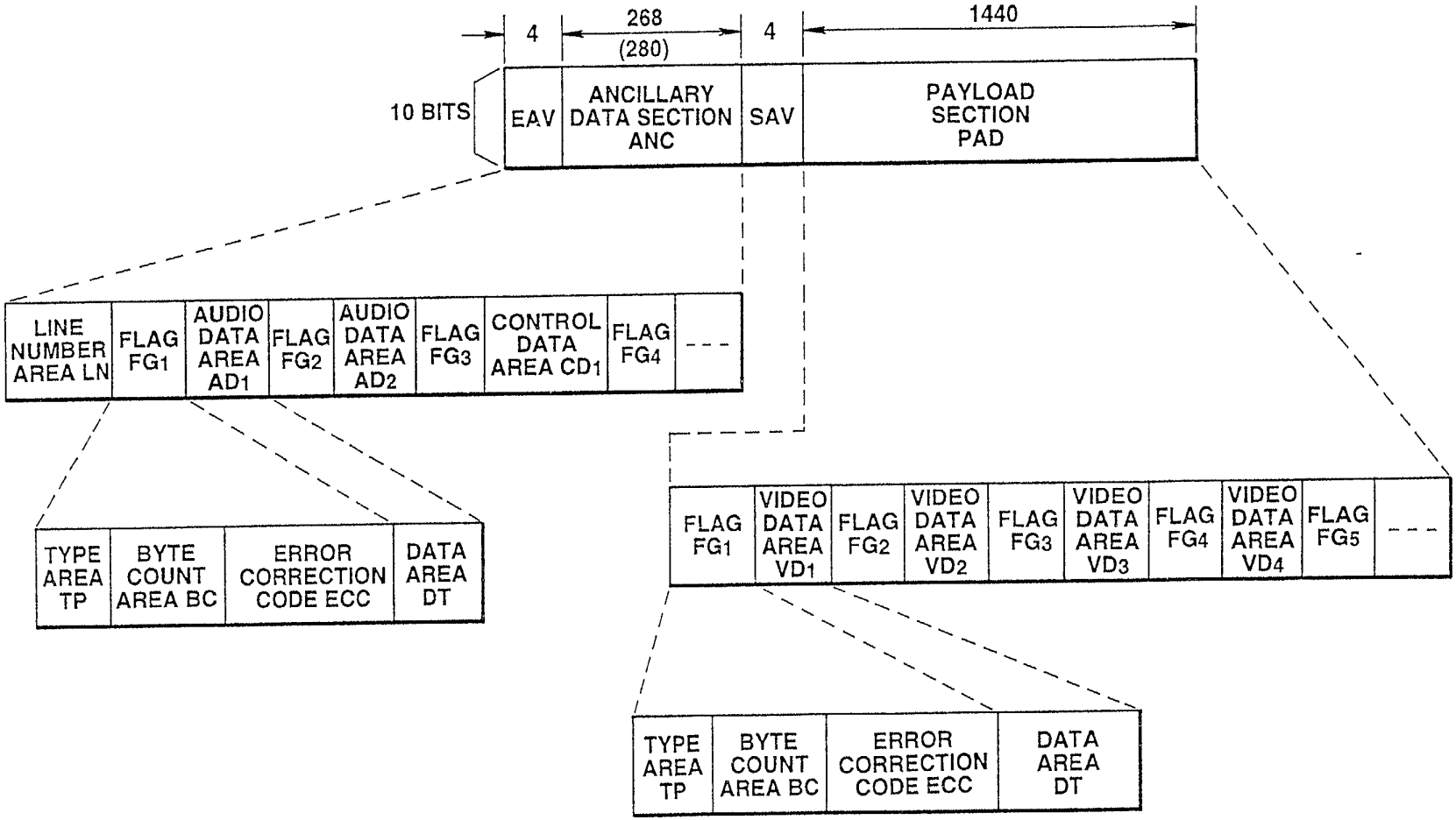
4
268
(280)
4
1440
10 BITS
EAV
ANCILLARY DATA SECTION ANC
SAV
PAYLOAD SECTION PAD
LINE NUMBER AREA LN
FLAG FG1
AUDIO DATA AREA AD1
FLAG FG2
AUDIO DATA AREA AD2
FLAG FG3
CONTROL DATA AREA CD1
FLAG FG4
TYPE AREA TP
BYTE COUNT AREA BC
ERROR CORRECTION CODE ECC
DATA AREA DT
FLAG FG1
VIDEO DATA AREA VD1
FLAG FG2
VIDEO DATA AREA VD2
FLAG FG3
VIDEO DATA AREA VD3
FLAG FG4
VIDEO DATA AREA VD4
FLAG FG5
TYPE AREA TP
BYTE COUNT AREA BC
ERROR CORRECTION CODE ECC
DATA AREA DT

FIG.3

	9(MSB)	8	7	6	5	4	3	2	1	0(LSB)
LINE NUMBER AREA LN	/8	P	LCT	LN6	LN5	LN4	LN3	LN2	LN1	LN0

FIG.4A

	9(MSB)	8	7	6	5	4	3	2	1	0(LSB)
TYPE AREA TP	/8	P	TCT	T6	T5	T4	T3	T2	T1	T0

FIG.4B

	9(MSB)	8	7	6	5	4	3	2	1	0(LSB)
BYTE COUNT AREA BC	/8	P	BCT	BC6	BC5	BC4	BC3	BC2	BC1	BC0

FIG.4C

	9(MSB)	8	7	6	5	4	3	2	1	0(LSB)
LINE NUMBER AREA LN	/8	P	0	LN6	LN5	LN4	LN3	LN2	LN1	LN0

FIG.5A

	9(MSB)	8	7	6	5	4	3	2	1	0(LSB)
LINE NUMBER AREA LN_1	/8	P	1	LN6	LN5	LN4	LN3	LN2	LN1	LN0
LINE NUMBER AREA LN_2	/8	P	0	LN13	LN12	LN11	LN10	LN9	LN8	LN7

FIG.5B

	9(MSB)	8	7	6	5	4	3	2	1	0(LSB)
LINE NUMBER AREA LN_1	/8	P	1	LN6	LN5	LN4	LN3	LN2	LN1	LN0
LINE NUMBER AREA LN_2	/8	P	1	LN13	LN12	LN11	LN10	LN9	LN8	LN7
LINE NUMBER AREA LN_3	/8	P	0	LN20	LN19	LN18	LN17	LN16	LN15	LN14

FIG.5C

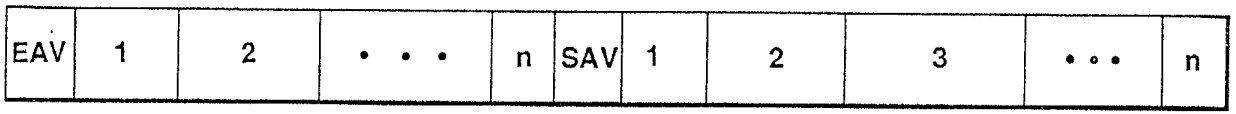

FIG.6A

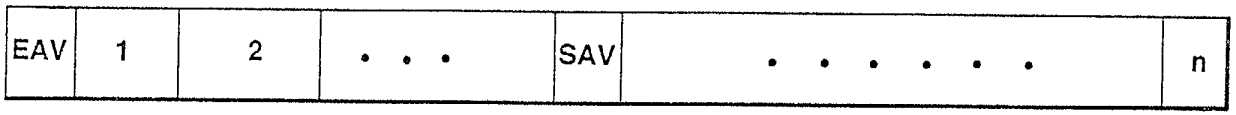

FIG.6B

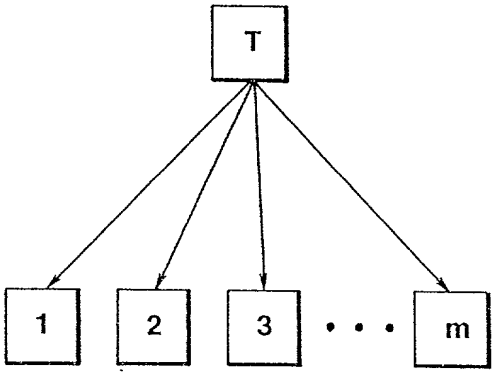

FIG.7A

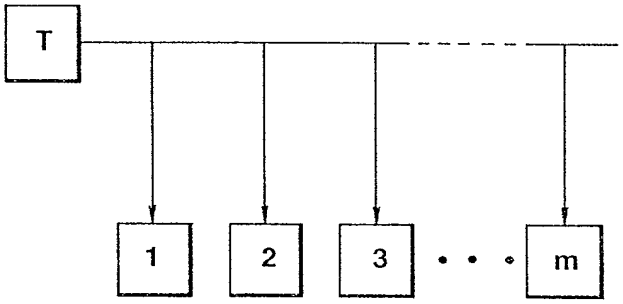

FIG.7B

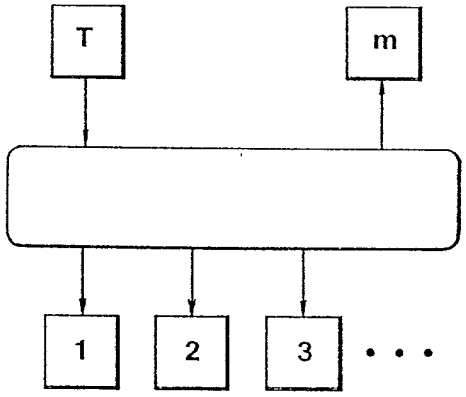

FIG.7C

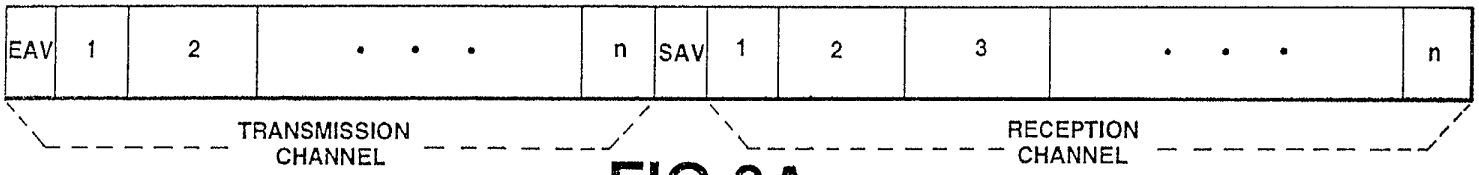
EAV
1
2
• • •
n
SAV
1
2
3
• • •
n
TRANSMISSION CHANNEL
RECEPTION CHANNEL

FIG.8A

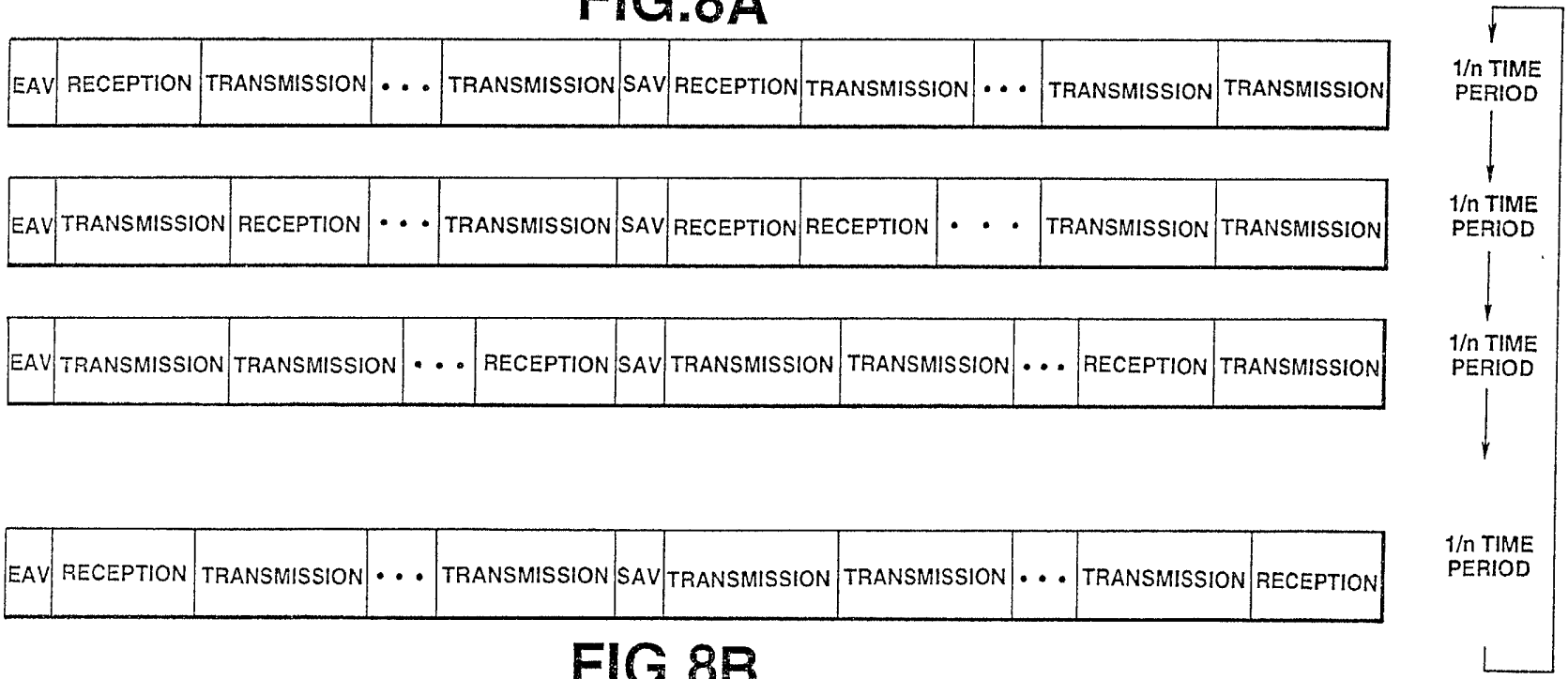
EAV RECEPTION TRANSMISSION • • • TRANSMISSION SAV RECEPTION TRANSMISSION • • • TRANSMISSION TRANSMISSION
EAV TRANSMISSION RECEPTION • • • TRANSMISSION SAV RECEPTION RECEPTION • • • TRANSMISSION TRANSMISSION
EAV TRANSMISSION TRANSMISSION • • • RECEPTION SAV TRANSMISSION TRANSMISSION • • • RECEPTION TRANSMISSION
EAV RECEPTION TRANSMISSION • • • TRANSMISSION SAV TRANSMISSION TRANSMISSION • • • TRANSMISSION RECEPTION
1/n TIME PERIOD
1/n TIME PERIOD
1/n TIME PERIOD
1/n TIME PERIOD

FIG.8B

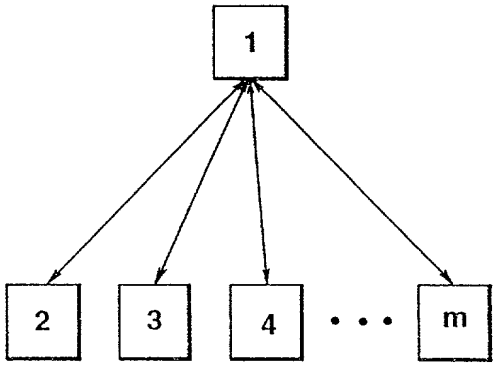

FIG.9A

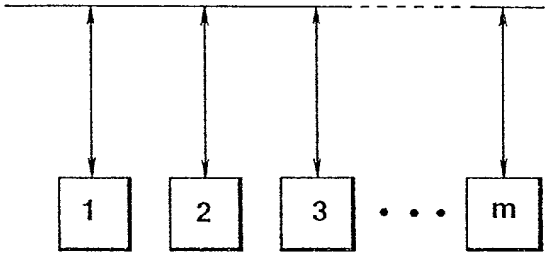

FIG.9B

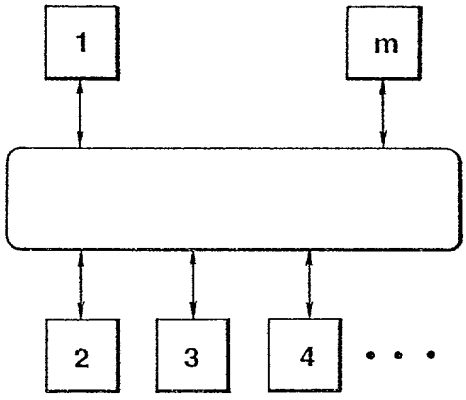

FIG.9C

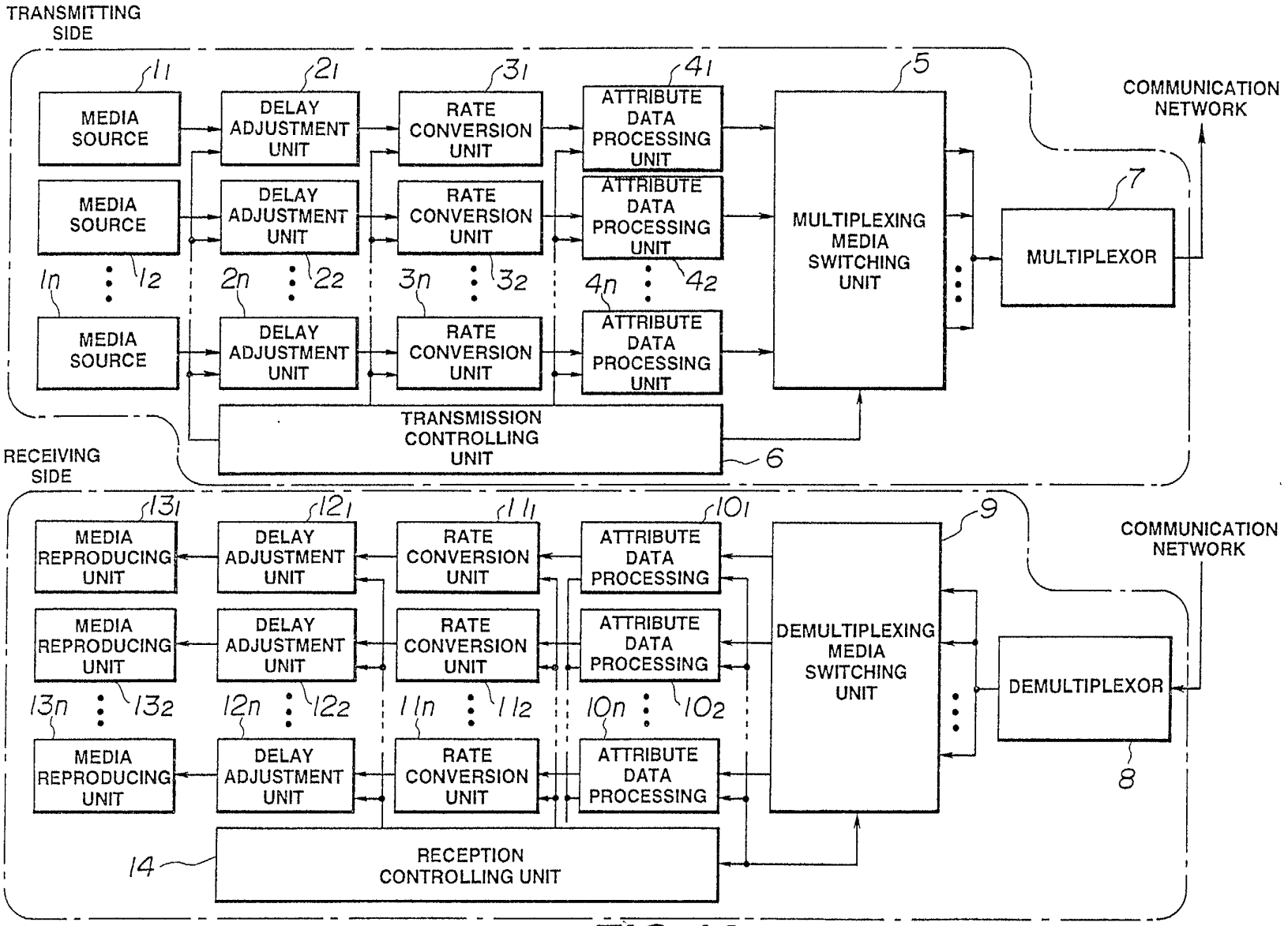
TRANSMITTING SIDE
11
21
31
41
5
MEDIA SOURCE
DELAY ADJUSTMENT UNIT
RATE CONVERSION UNIT
ATTRIBUTE DATA PROCESSING UNIT
MULTIPLEXING MEDIA SWITCHING UNIT
COMMUNICATION NETWORK
7
MULTIPLEXOR
1n
12
2n
22
3n
32
4n
42
TRANSMISSION CONTROLLING UNIT
6
RECEIVING SIDE
131
121
111
101
9
MEDIA REPRODUCING UNIT
DEMULTIPLEXING MEDIA SWITCHING UNIT
DEMULTIPLEXOR
13n
132
12n
122
11n
112
10n
102
8
14
RECEPTION CONTROLLING UNIT

FIG.10

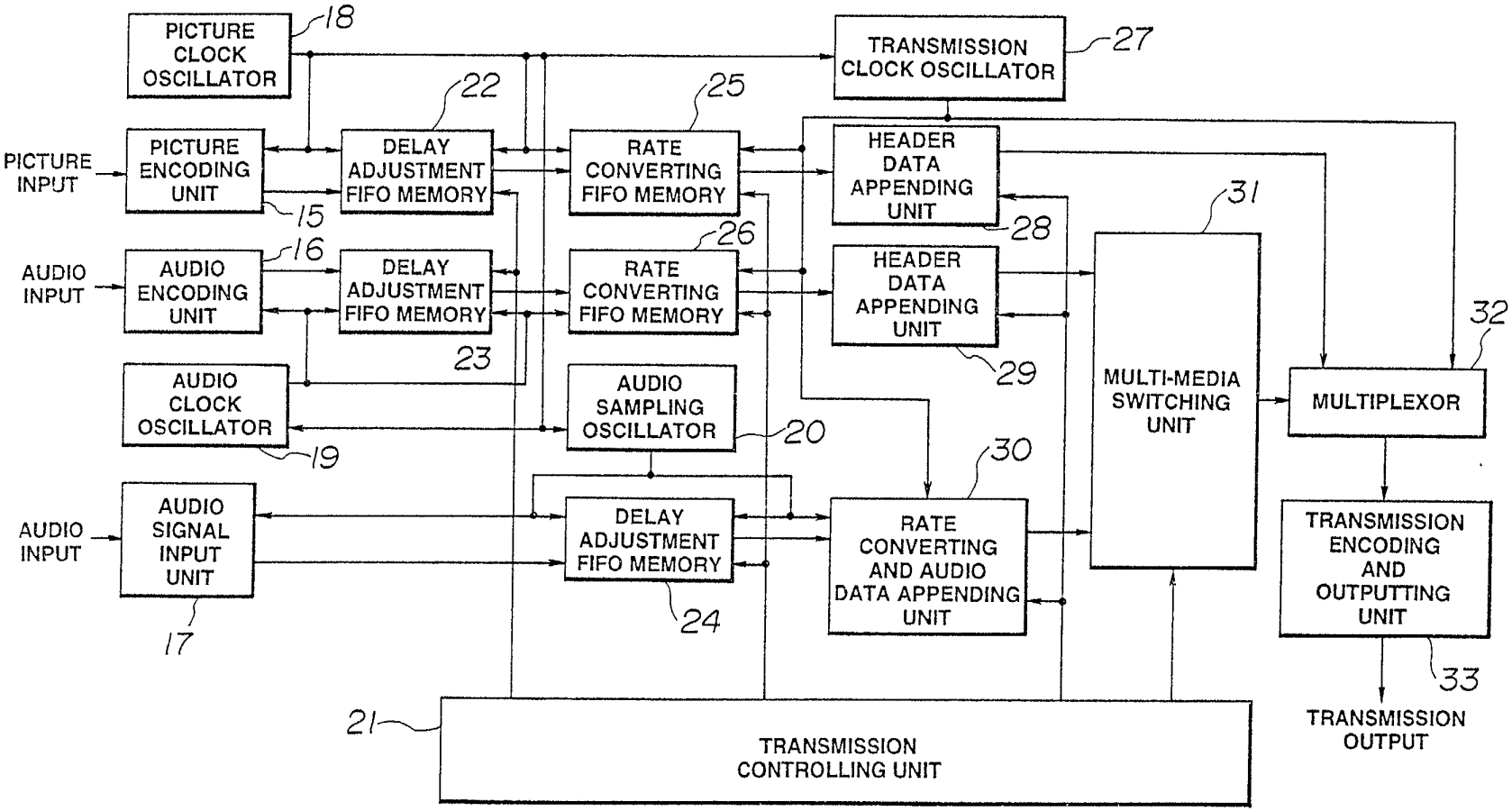
PICTURE CLOCK OSCILLATOR
18
TRANSMISSION CLOCK OSCILLATOR
27
22
25
PICTURE INPUT
PICTURE ENCODING UNIT
15
DELAY ADJUSTMENT FIFO MEMORY
RATE CONVERTING FIFO MEMORY
HEADER DATA APPENDING UNIT
28
31
AUDIO INPUT
16
AUDIO ENCODING UNIT
DELAY ADJUSTMENT FIFO MEMORY
26
RATE CONVERTING FIFO MEMORY
HEADER DATA APPENDING UNIT
29
32
23
AUDIO CLOCK OSCILLATOR
19
AUDIO SAMPLING OSCILLATOR
20
MULTI-MEDIA SWITCHING UNIT
MULTIPLEXOR
30
AUDIO INPUT
AUDIO SIGNAL INPUT UNIT
17
DELAY ADJUSTMENT FIFO MEMORY
24
RATE CONVERTING AND AUDIO DATA APPENDING UNIT
TRANSMISSION ENCODING AND OUTPUTTING UNIT
33
TRANSMISSION OUTPUT
21
TRANSMISSION CONTROLLING UNIT

FIG.11

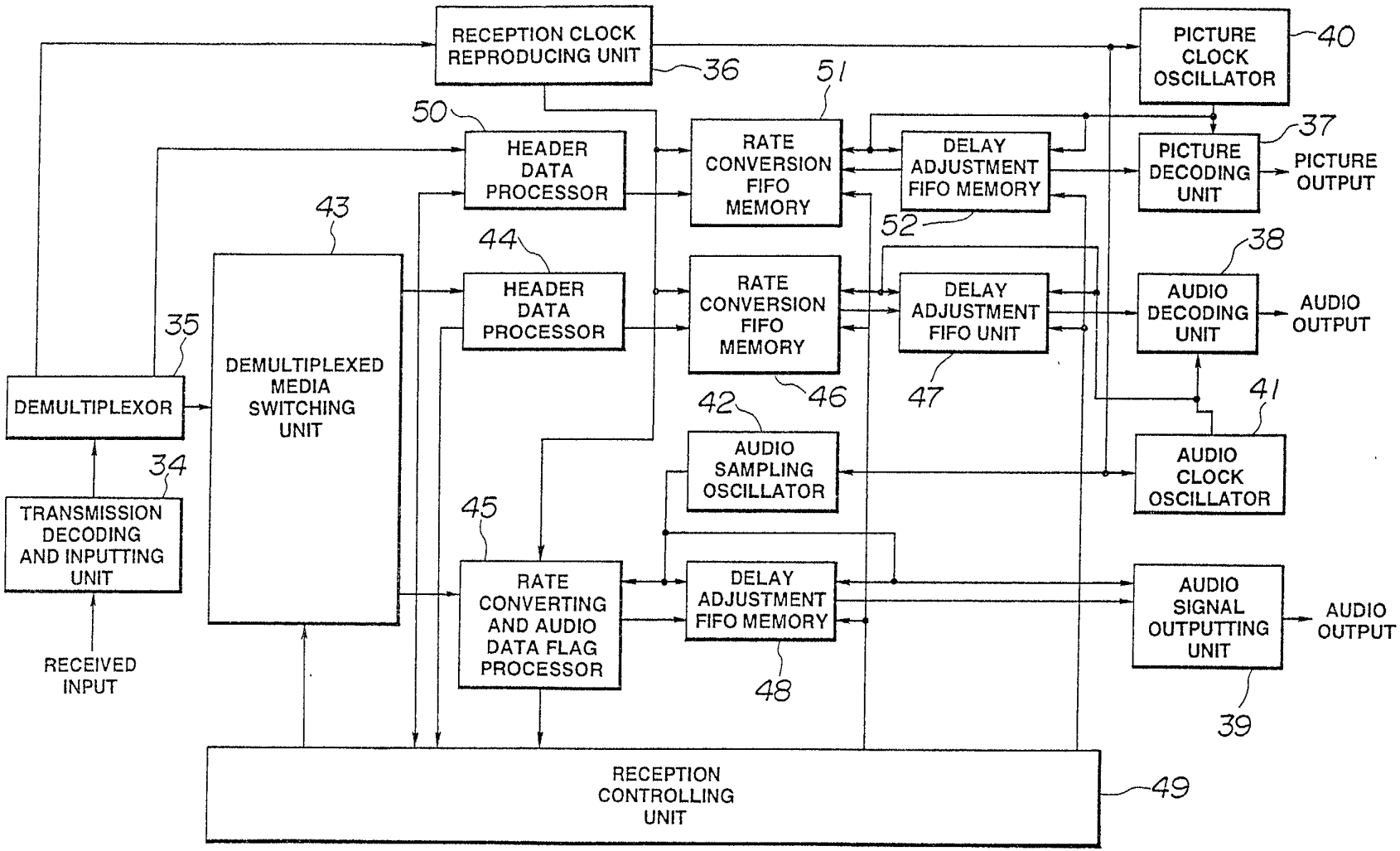
RECEPTION CLOCK REPRODUCING UNIT
36
PICTURE CLOCK OSCILLATOR
40
50
HEADER DATA PROCESSOR
51
RATE CONVERSION FIFO MEMORY
DELAY ADJUSTMENT FIFO MEMORY
37
PICTURE DECODING UNIT
PICTURE OUTPUT
52
43
44
HEADER DATA PROCESSOR
RATE CONVERSION FIFO MEMORY
38
AUDIO DECODING UNIT
AUDIO OUTPUT
35
DEMULTIPLEXOR
DEMULTIPLEXED MEDIA SWITCHING UNIT
DELAY ADJUSTMENT FIFO UNIT
46
47
41
42
AUDIO SAMPLING OSCILLATOR
AUDIO CLOCK OSCILLATOR
34
TRANSMISSION DECODING AND INPUTTING UNIT
45
RATE CONVERTING AND AUDIO DATA FLAG PROCESSOR
DELAY ADJUSTMENT FIFO MEMORY
AUDIO SIGNAL OUTPUTTING UNIT
AUDIO OUTPUT
48
39
RECEIVED INPUT
RECEPTION CONTROLLING UNIT
49

FIG.12

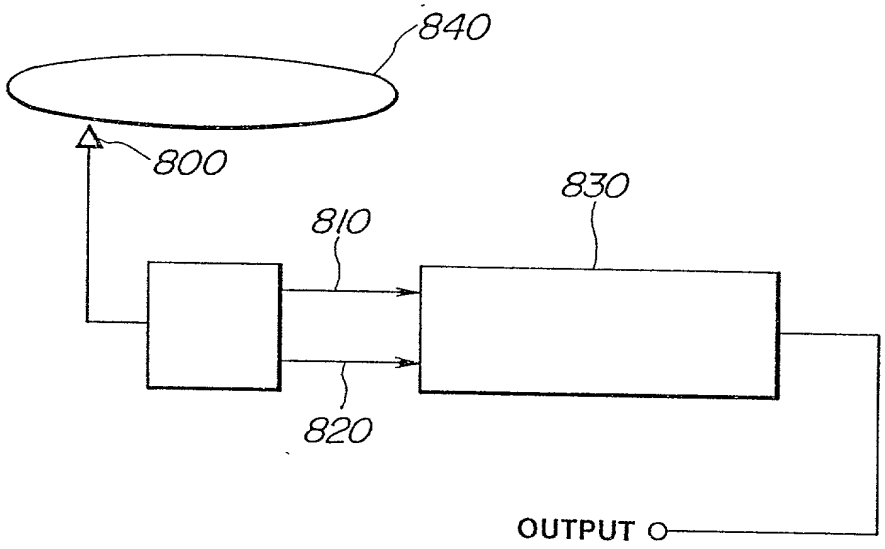

FIG.13

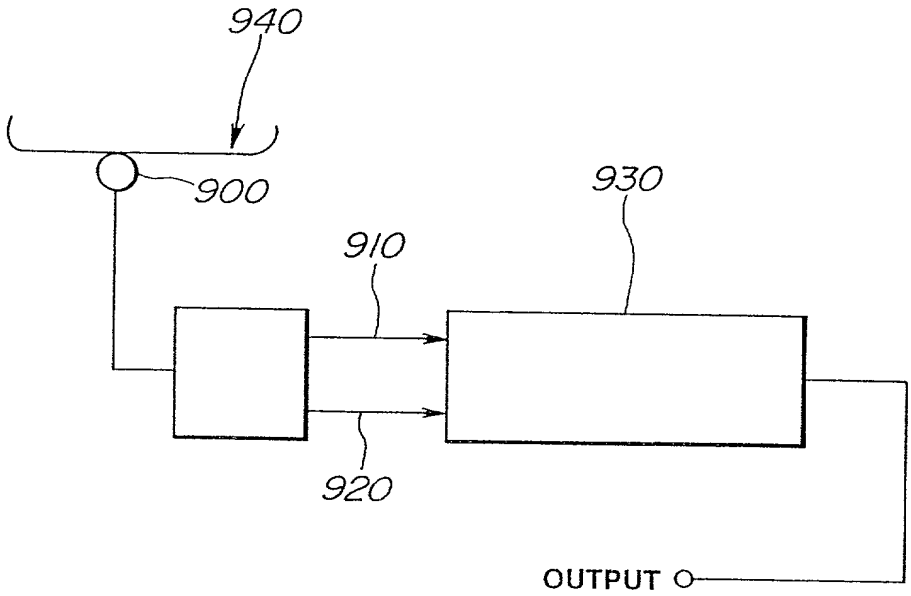

FIG.14

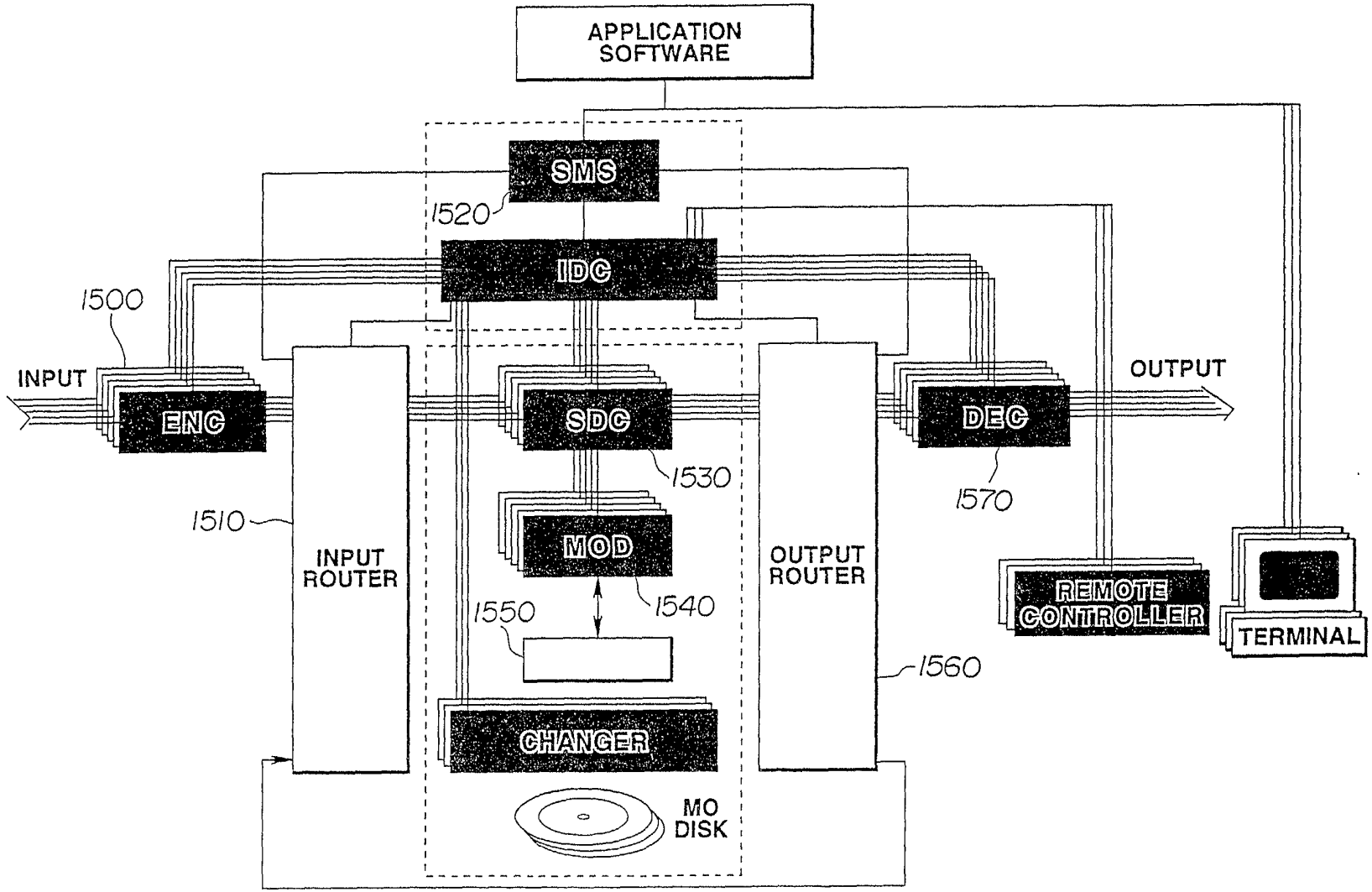
APPLICATION SOFTWARE
SMS
1520
IDC
1500
INPUT
ENC
SDC
1530
DEC
OUTPUT
1570
1510
INPUT ROUTER
MOD
1540
1550
OUTPUT ROUTER
REMOTE CONTROLLER
TERMINAL
1560
CHANGER
MO DISK

FIG.15

Declaration and Power of Attorney For Patent Application

特許出願宣言書

Japanese Language Declaration

私は、下欄に氏名を記載した発明者として、以下のことを宣言する。

As a below named inventor, I hereby declare that:

私の住所、郵便の宛先および国籍は、下欄に氏名に続いて記載したとおりであり、

My residence, post office address and citizenship are as stated below next to my name,

名称の発明に関し、請求の範囲に記載した特許を求める主題の本来の、最初にして唯一の発明者である（一人の氏名のみが下欄に記載されている場合）か、もしくは本来の、最初にして共同の発明者である（複数の氏名が下欄に記載されている場合）と信じ、

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Digital Serial Data Interface

その明細書を
（該当する方に印を付す）

the specification of which

(check one)

☐ ここに添付する。

☐ is attached hereto.

☒ _____日に出願番号

☒ was filed on 6/22/95 as

第 _____ 号として提出し、

Application Serial No. 08/493,732

_____ 日に補正した。
（該当する場合）

and was amended on _____
(if applicable)

私は、前記のとおり補正した請求の範囲を含む前記明細書の内容を検討し、理解したことを陳述する。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above

私は、連邦規則法典第37部第1章第56条（a）項に従い、本願の審査に所要の情報を開示すべき義務を有することを認める。

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a)

Japanese Language Declaration

私は、合衆国法典第35部第119 条にもとづく下記の外国特許出願または発明者証出願の外国優先権利益を主張し、さらに優先権の主張に係る基礎出願の出願日前の出願日を有する外国特許出願または発明者証出願を以下に明記する：

I hereby claim foreign priority benefits under Title 35 United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior foreign applications
先の外国出願

			Priority claimed 優先権の主張
06-144403 (Number) 番号	Japan (Country) 国名	27/June/1994 (Day Month Year Filed) 出願の年月日	~~Yes~~ No はい いいえ
(Number) 番号	(Country) 国名	(Day Month Year Filed) 出願の年月日	Yes No はい いいえ
(Number) 番号	(Country) 国名	(Day Month Year Filed) 出願の年月日	Yes No はい いいえ

私は、合衆国法典第35部第120 条にもとづく下記の合衆国特許出願の利益を主張し、本願の請求の範囲各項に記載の主題が合衆国法典第35部第112 条第1項に規定の態様で先の合衆国出願に開示されていない限度において、先の出願の出願日と本願の国内出願日またはＰＣＴ国際出願日の間に公表された連邦規則法典第37部第1章第56条（a）項に記載の所要の情報を開示すべき義務を有することを認める：

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37 Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) 出願番号	(Filing Date) 出願日	(現況) 特許済み、係属中、放棄済み	Status (patented pending abandoned)
(Application Serial No.) 出願番号	(Filing Date) 出願日	(現況) 特許済み、係属中、放棄済み	Status (patented pending abandoned)

私は、ここに自己の知識にもとづいて行った陳述がすべて真実であり、自己の有する情報および信ずるところに従って行った陳述が真実であると信じ、さらに故意に虚偽の陳述等を行った場合、合衆国法典第18部第1001条により、罰金もしくは禁錮に処せられるか、またはこれらの刑が併科され、またかかる故意による虚偽の陳述が本願ないし本願に対して付与される特許の有効性を損うことがあることを認識して、以上の陳述を行ったことを宣誓する。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration

委任状：私は、下記発明者として、以下の代理人をここに選任し、本願の手続を遂行すること並びにこれに関する一切の行為を特許商標庁に対して行うことを委任する代理人氏名および登録番号を明記のこと。

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (*list name and registration number*)

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Shawn L. McClintock	31,980
Robert P. Biddle	35,826
Pasquale Musacchio	36,876
Peter C. Toto	36,293
Lise A. Rode	37,226

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Direct Telephone Calls to: (*name and telephone numoer*)

Jerry A. Miller - (201)930-7315

単一のまたは第一の発明者の氏名	Full name of sole or first inventor Naoki Fujisaki
単発明者の署名　日付	Inventor's signature　Date Naoki Fujisaki　September 25, 1991
住所	Residence Kanagawa, Japan
国籍	Citizenship Japan
郵便の宛先	Post Office Address Sony Corporation
	7-35, Kitashinagawa 6-Chome, Shinagawa-Ku, Tokyo, Japan
第２の共同発明者の氏名（該当する場合）	Full name of second joint inventor, if any
同第２発明者の署名　日付	Second inventor's signature　Date
住所	Residence
国籍	Citizenship
郵便の宛先	Post Office Address

（第六またはそれ以降の共同発明者に対しても同様な情報および署名を提供すること。）

(Supply similar information and signature for third and subsequent joint inventors.)